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Abstract
Fast Fourier Transform (FFT) has been the most important functions widely used in the Multi-Band Orthogonal Frequency Division Multiplexing Ultra-Wide Band (MB-OFDM UWB) system and image compression, especially in the exponential growth of mobile and handheld devices. The higher throughput requirements for video broadcasting and wireless network will consume ever more power. Since Fast Fourier Transform algorithm was first proposed in 1965 by Cooley-Tuke and promoted the development in the areas of digital communication, the design of FFT hardware has also evolved from the pipeline to the parallel-pipeline structure. This thesis will be contributing on proposing a new parallel-pipeline structure to the Multiple-Path Delay Commutator (MDC), that will have double rate of the FFT operation, achieve 100% hardware utility rate and at the same time reduce the hardware area, and produce parallel-input and parallel-output that can be applied to the MIMO system. In addition, the new parallel structure can also be applied on more communication systems. The ultimate goal of this thesis is to use the new parallel-pipeline structure to realize a FFT mechanism that conforms to the IEEE 802.15.3a standard of high performance, high efficiency, low delay, and low power and also implementation complete circuit simulation and verification utilizing Xilinx Virtex-4-xc4vlx60 FPGA.
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